The DØ Silicon Track Trigger

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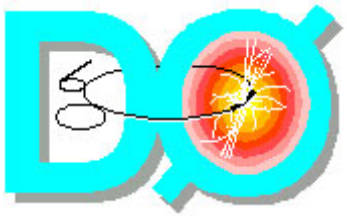
Collaboration Meeting 10/11/2002

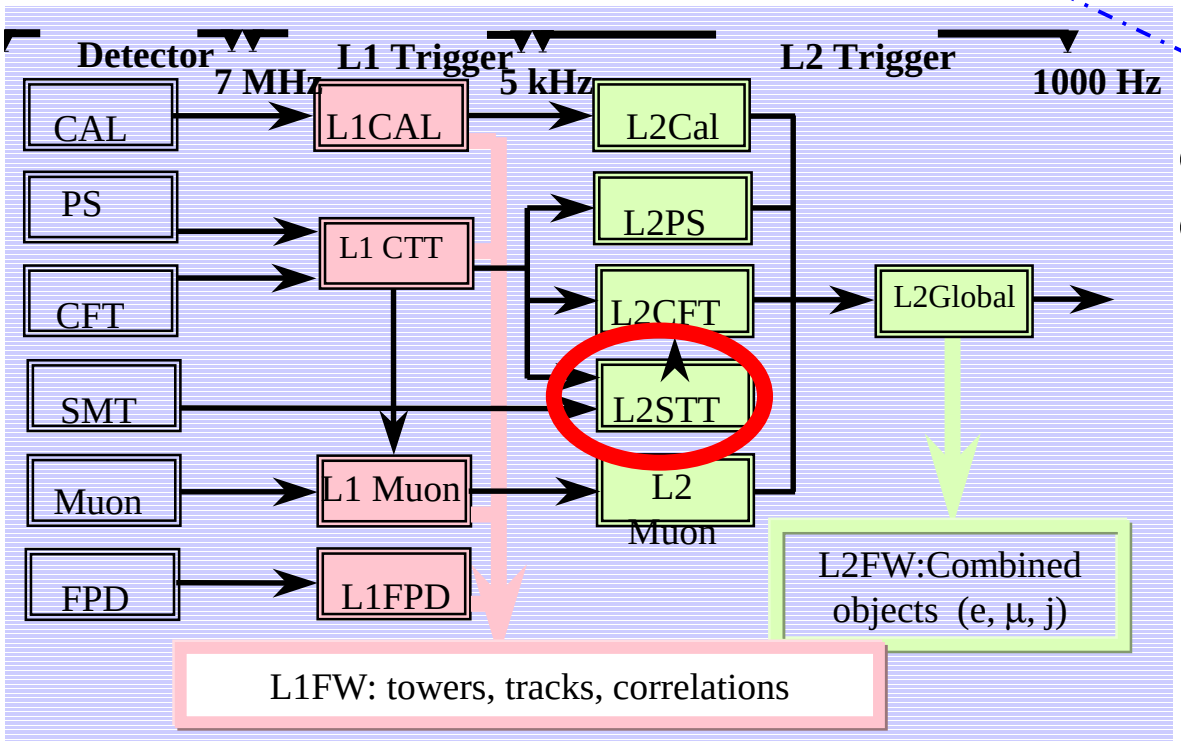


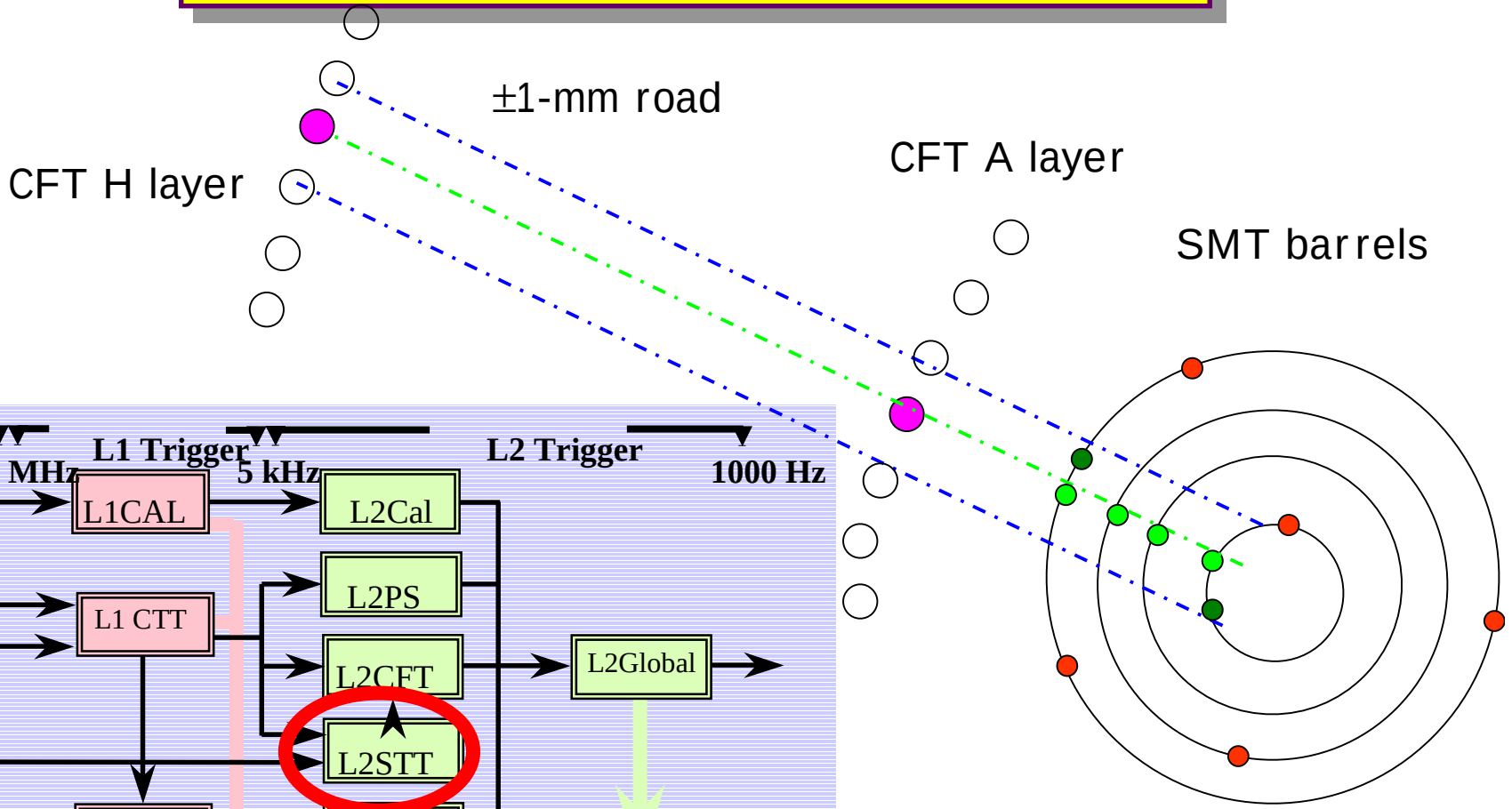
- **Introduction**
- **Design**
- **Status**
- **Schedule**

Physics Motivation

- **Increase inclusive bb production yield six-fold with low enough threshold to see Z→bb signal**
  - **Control sample for b-jet energy calibration, bb mass resolution, b trigger and tagging efficiencies**
- **Top quark physics**
  - **Factor of 2 improvement in top mass resolution due to improved jet energy scale calibration**
- **Heavy bb resonances for Higgs searches**
  - **Double trigger efficiency for ZH→(νν)(bb) by rejecting QCD gluons and light-quark jets**
- **b-quark physics**
  - **Lower p_T threshold on single lepton and dilepton triggers (B^o→μμ, B_s mixing, etc.)**
  - **Increase B_d^o→J/Ψ $K_S$yield by 50% (CP violation)**

STT Overview



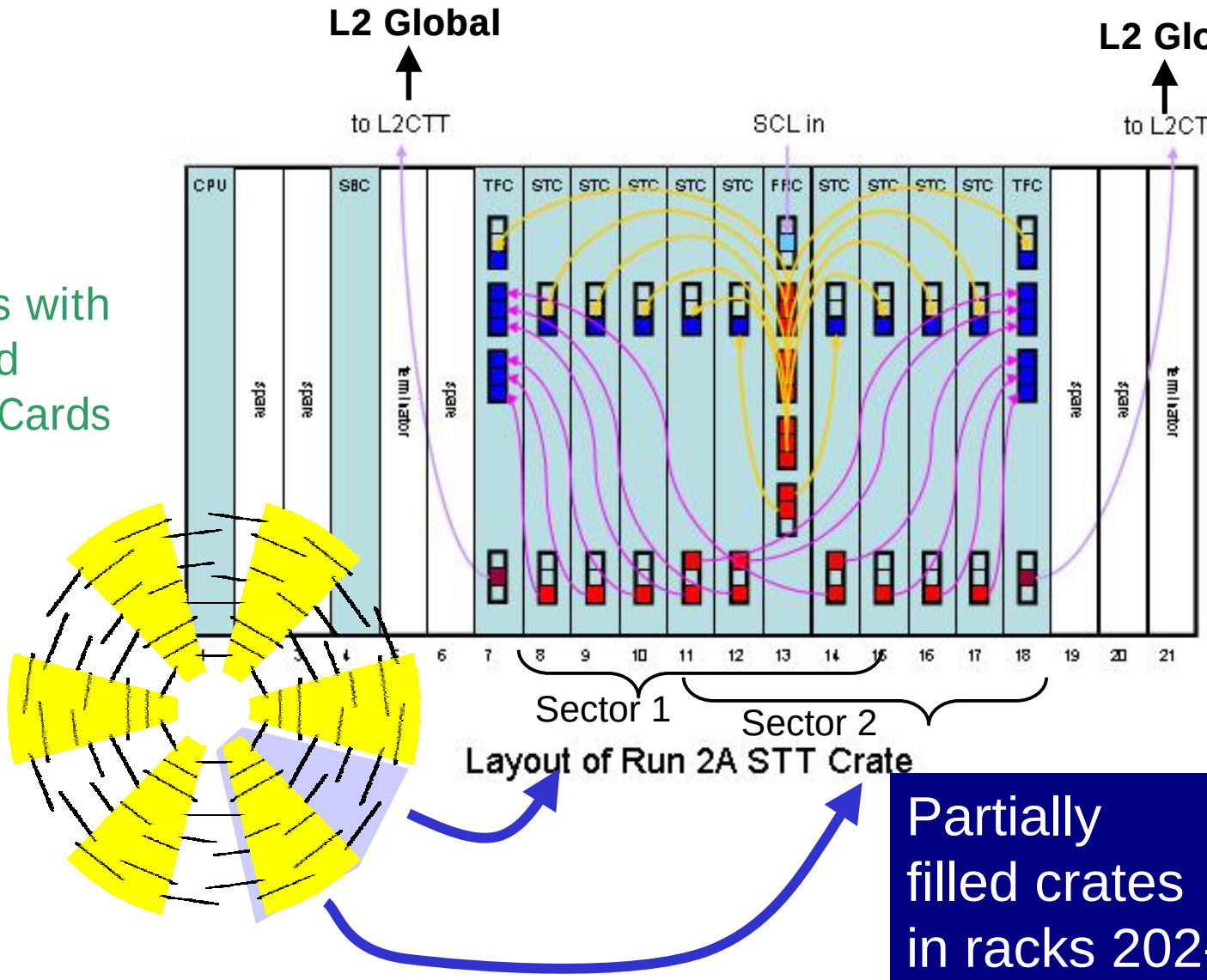


Contributing Institutions

- **Boston University**
  - U. Heintz, M. Narain, E. Popkov (PD), L. Sonnenschein (PD), J. Wittlin (PD), K. Black (GS), S. Fatakia (GS), A. Zabi (GS), Amitabha Das (GS), W. Earle (Eng), E. Hazen (Eng), S. Wu (Eng)
- **Columbia University**
  - H. Evans, G. Steinbrück (PD), T. Bose (GS), A. Qi (Eng)
- **Florida State University**
  - H. Wahl, H. Prosper, S. Linn, T. Adams, B. Lee (PD), S. Tentindo Repond (PD), S. Singupta (GS), J. Lazoflores (GS)
- **SUNY Stony Brook**
  - J. Hobbs, W. Taylor (PD), H. Dong (GS), C. Pancake (Eng), B. Smart (Eng), J. Wu (Eng)
- **Manchester University**
  - Michiel Sanders (PD)

STT Design

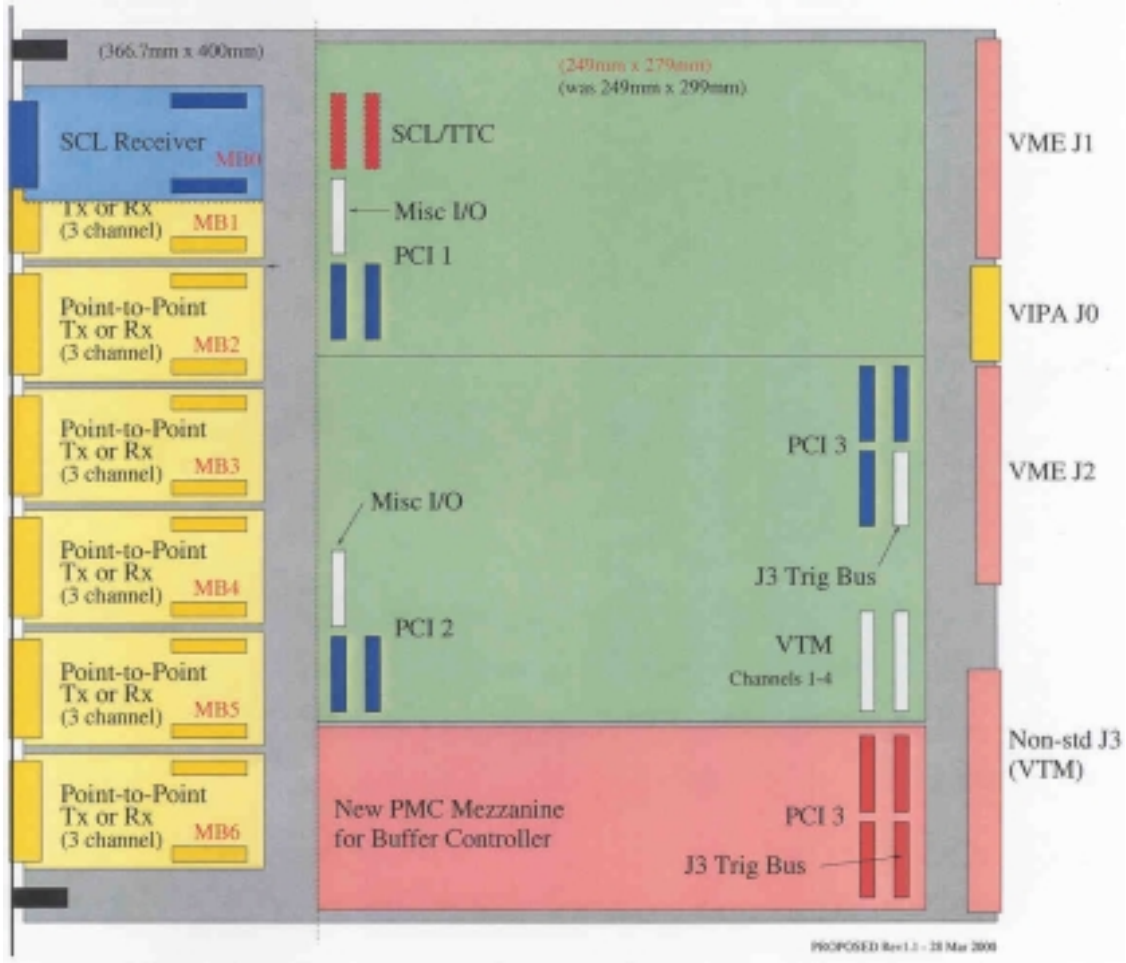
6 Identical Crates with
1 Fiber Road Card
9 Silicon Trigger Cards
2 Track Fit Cards



Partially filled crates in racks 202-204 in MCH2

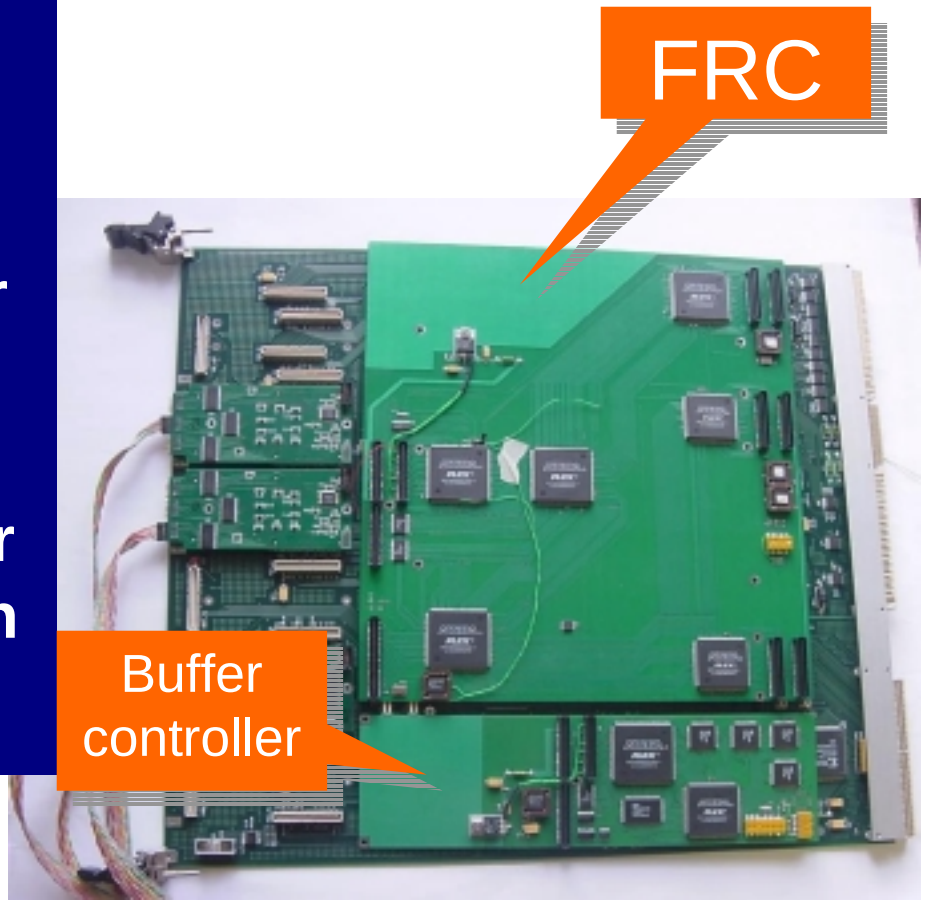
Motherboard and Communication Links

- Boston University
- 9Ux400 mm VME64x-compatible
- 3 33-MHz PCI busses for on-board communications
- Data communicated between cards via point-to-point links (LVDS) (LTB and LRB cards)
- Control signals sent over backplane using dedicated lines
- VME bus used for Level 3 readout and initialization/monitoring



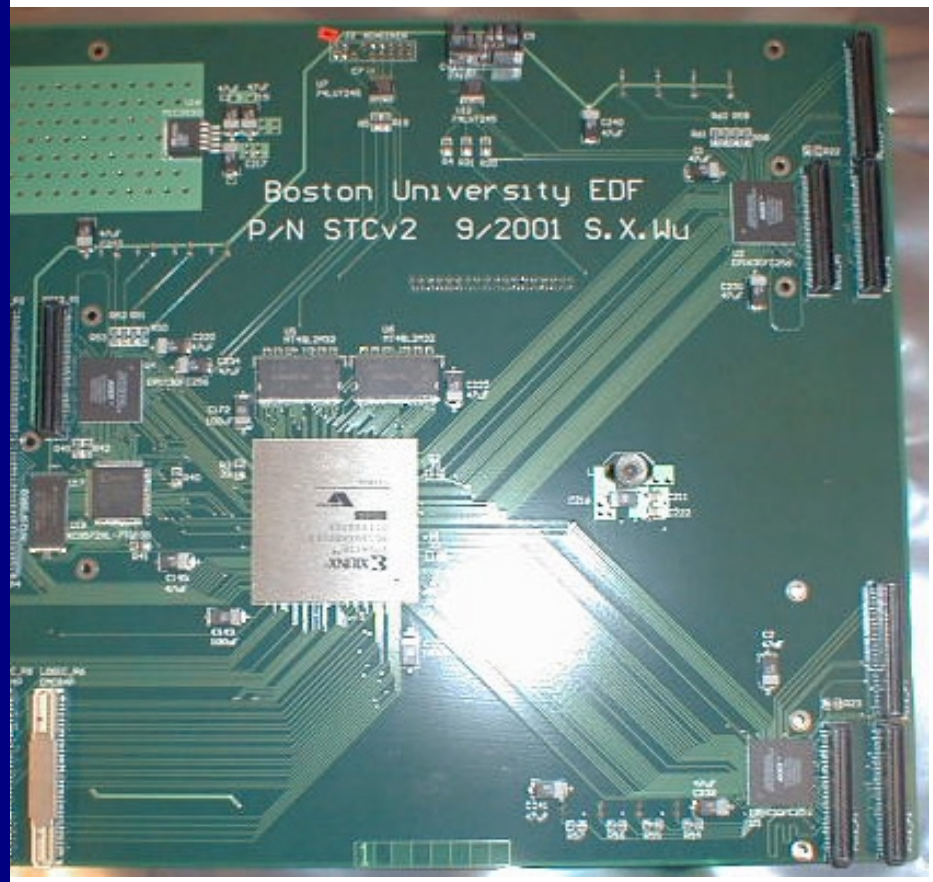
Fiber Road Card (FRC) Design

- Columbia University
- Receives tracks from L1CTT
- Communicates with trigger framework via SCL receiver card
- Transmits tracks and trigger info to other cards
- Manages L3 buffering and readout via Buffer Controller (BC) daughter cards on each motherboard



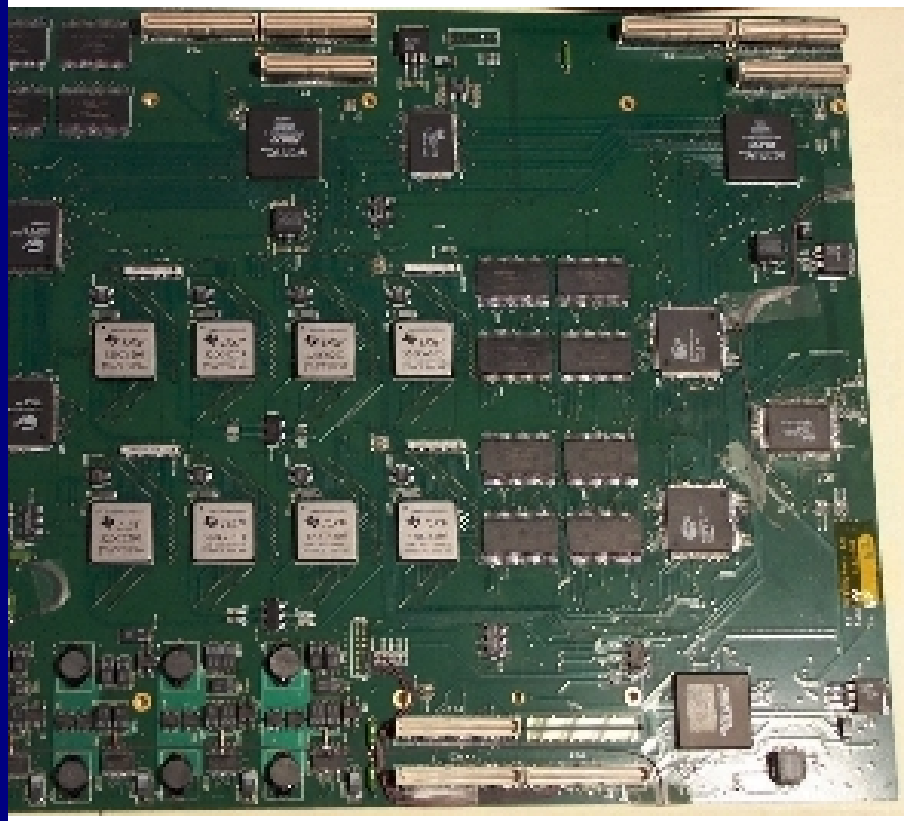
Silicon Trigger Card (STC) Design

- Boston University
- Performs SMT clustering and cluster-road matching
  - Clusters Neighbouring SMT hits (axial and stereo)
  - Each STC processes 8 HDI inputs simultaneously
  - Axial clusters are matched to ±1mm-wide roads around each CFT track via precomputed LUT
  - Mask bad strips and apply pedestal/gain corrections (via LUTs)



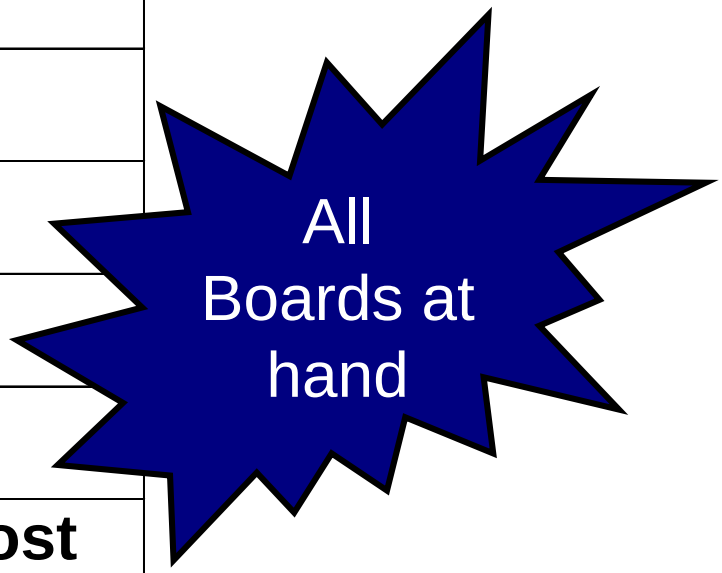
Track Fit Card (TFC) Design

- SUNY Stony Brook
- Performs final SMT cluster filtering and track fitting
  - Receives 2 CFT hits and axial SMT clusters in CFT road
  - Lookup table used to convert hardware to physical coordinates
  - Selects clusters closest to road center and performs linearized track fit using precomputed matrix elements stored in on-board LUT
  - Require only 3 hits out of 4
- Output to L2CTT via Hotlink cards



Hardware Status

	Need	Have	Spares
FRC	6	➨	3
STC	54	➨	6
TFC	12	➨	3
BC	72	➨	19
MB	72	➨	
LRB/LTB	168	➨	
Hotlink X	12	➨	
VTMs	60	➨	5, 7 lost to D0!



Downloading and Monitoring

- Florida State University and Boston University
- STT Crate Initialization
  - Controlled via Power PC at power-up
  - Downloads lookup tables and DSP code to STT cards
  - Existing test-mode uses Python; conversion to C for final system done for STC and TFC, in progress for FRC
- EPICS STT board support package
  - Downloads via COMICS trigger initialization parameters
  - Gathers information from cards for monitoring purposes
  - First pass exists
  - Needs to be extended
  - Need to implement Interrupt Service Routine to react to monitoring request via SCL→FRC→CPU

L2STTCTTWorker

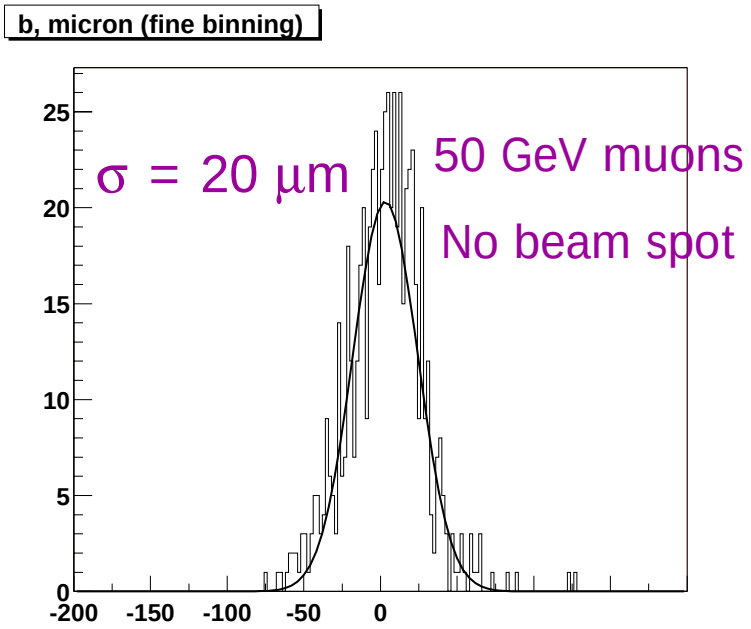
- Boston University
- **Online package (on alpha/ beta) that receives L2 STT output**
  - **Formats and orders it appropriately**
    - **combines the inputs from the 12 tfcs into 1 ordered list of ctt or stt+ctt tracks (depending on if there's a stt fit)**
    - **sorts by pt, does a few conversions (phi bins, pt bins, etc)**
  - **Transmits it to L2 Global for final L2 decision**

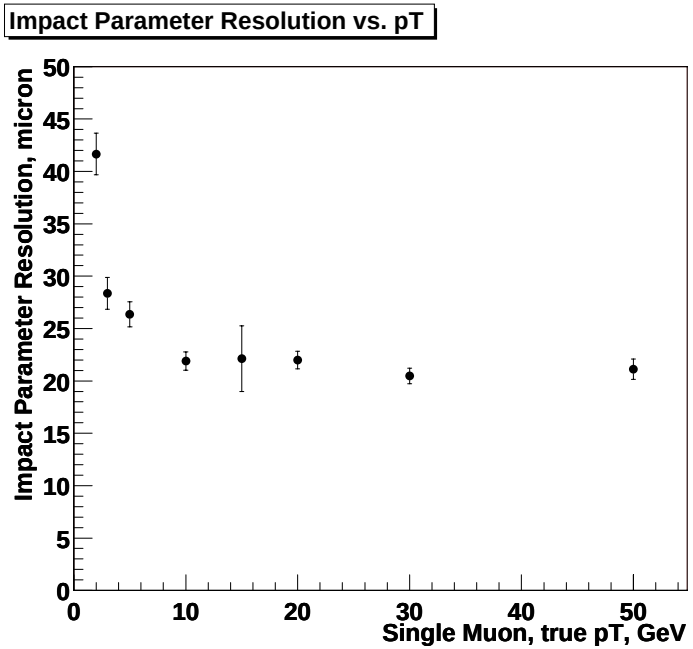
- **has been successfully tested with both 1 and 2 tfc's in standalone mode**
- **has been tested with full card chain for mult. Events**
- **Integrated into trigger simulator in p13**

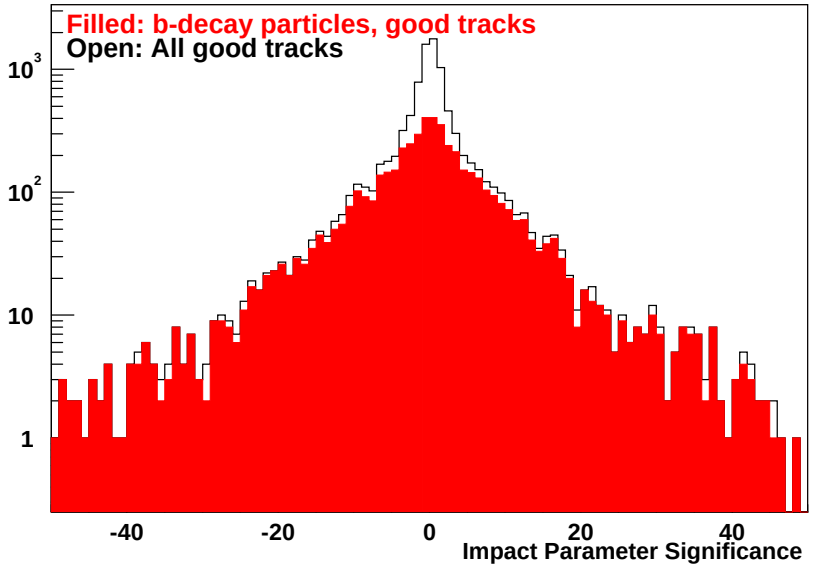
STT Trigger Simulator

- Florida State, Stony Brook and Boston University
- **Exact DSP fitting code used in tsim_l2stt**
- **Some ongoing development to improve the emulation of the hardware/firmware**
- **Has been instrumental in developing the fitting algorithm**
- **Produces test vectors for all cards**
- **Stand-alone package tsim_l2stt**
- **Very recently Integrated into d0trigsim→Can be used by the general (DØ) public for physics studies!**
- **Can be used with worker for physics studies.**

STT Performance







Beamspot Monitoring

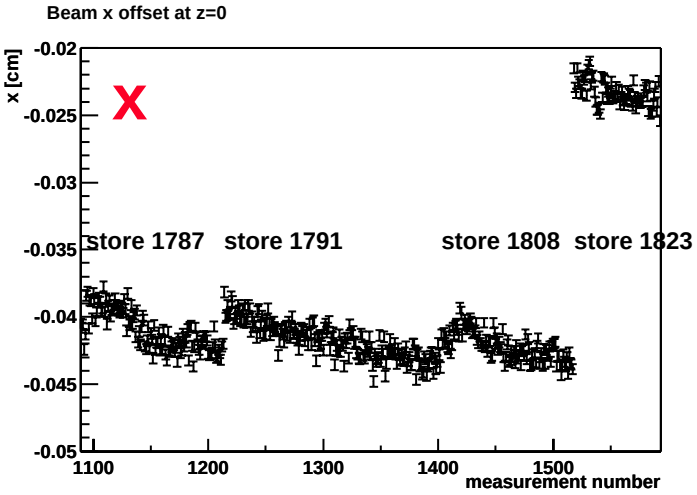
- Manchester University
- Use vertex examine to determine beam spot and vertices online
- Use gtr_l3 and Offline vertexing: Beam position from dca vs phi
- Write beam position to text file: ➨

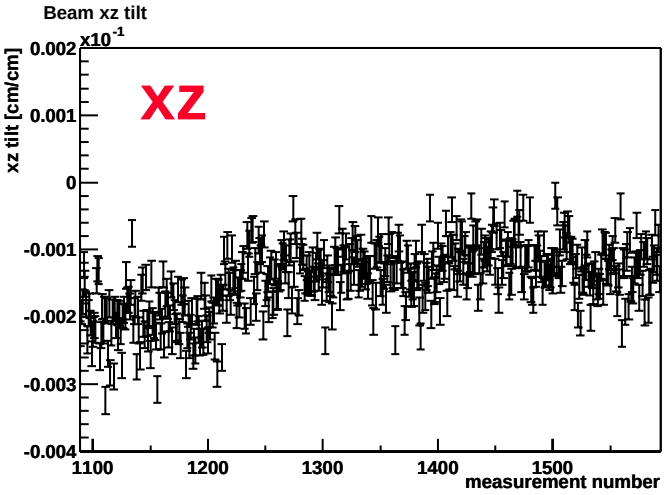
- Beam Monitor: (to do)
  - connected to Vertex examine, SES for alarms, Lumi system to get info →lumi db and acnet for feedback of beam spot to MCR
  - MCR could implement automatic beam adjustment
  - Writes beamspot to pickle file (updated every ~5 min)

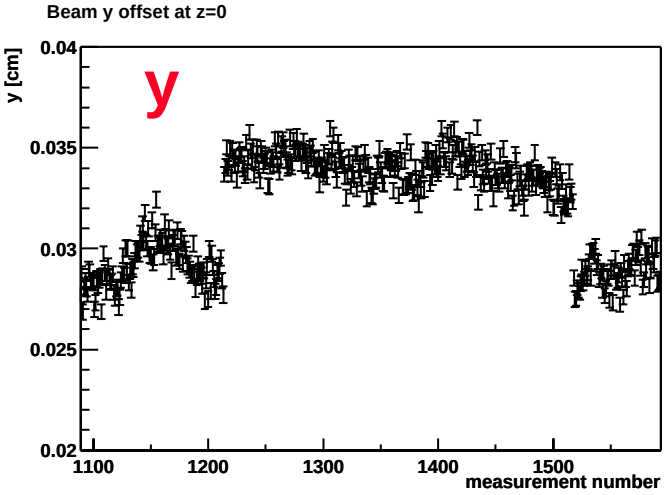
- TFC picks up beamspot from pickle file
- Picked up on start of new run (not yet)
- If beam moves too much→Alarm, stop run, start new run (new beam spot)
- Beam spot in beg of store: TBD
  - ~10 min to get measurement
  - Or: Special run with all L3 dedicated to tracking

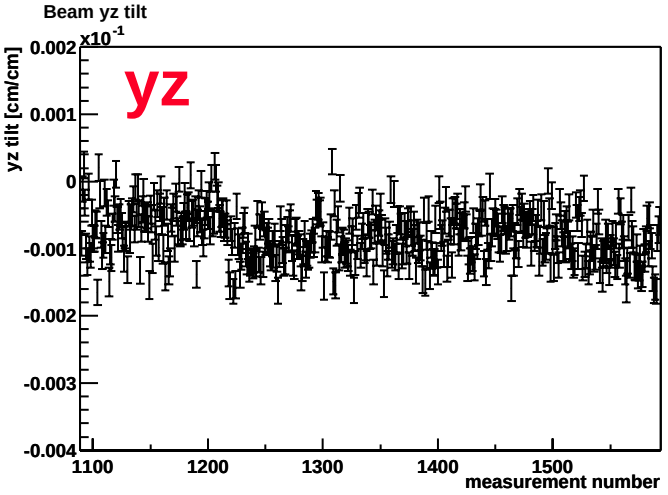
- thanks to Lorenzo and Suyong (beam_tilt / examine)

Beamspot Monitoring









Critical for the STT!

Integration Tests

- Used fake data sender (tracks to FRC and hits to STC) to verify transfers between all 3 types of boards
- Fake data sender triggered by L1 accepts: Have started to test integration of FRC with SCL signals ✪
- Next step: tick and turn number in fake CTT data
- Loaded FRC and STC with test vectors and sent multiple events through FRC->STC->TFC->L2 alpha chain ✪
- Ongoing: Rate tests using fake data sender
- L3 readout involving FRC $\rightarrow$ BC communication in progress
- Real CTT tracks and Silicon hits will be used as soon as L1CTT tracks available!

30° Sector test

- Instrumenting a 30° sector:
  - One FRC, 6 STC's, one TFC
- Full track reconstruction
- parasitic operation
- Output to L3 and private DAQ for L2

- Status: All hardware at hand at FNAL
- Transition from Integration tests to sector test ongoing
- Work on L3 readout ongoing

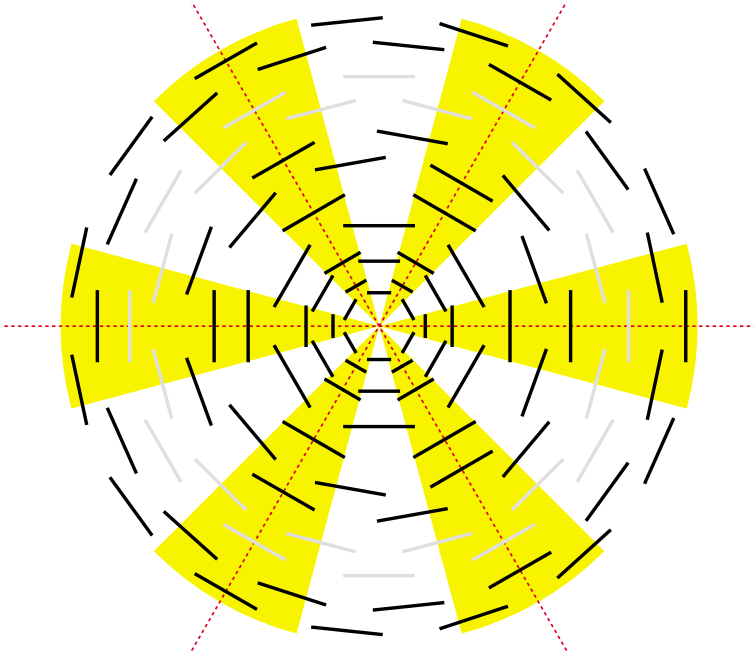
Schedule

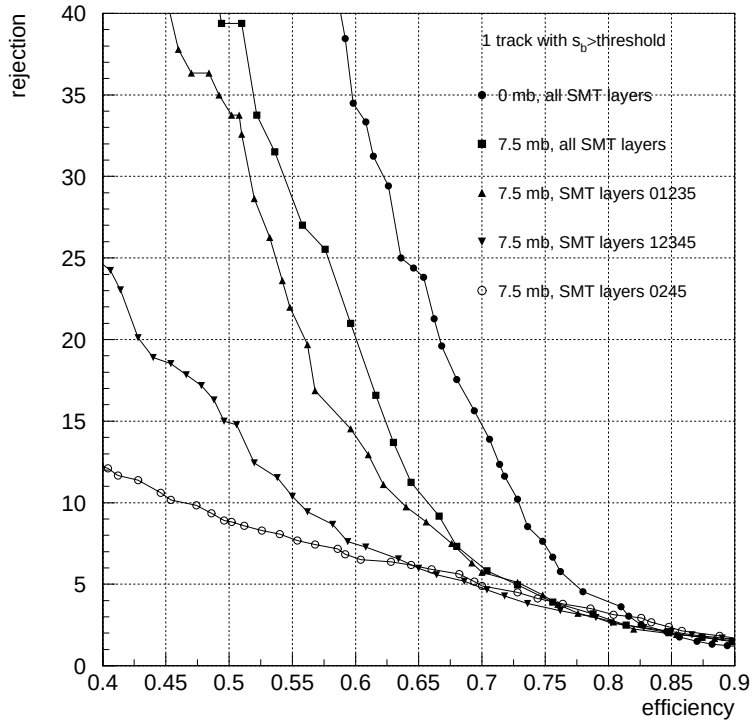
- Production ➨
- Installation 1 week (beg of November) No access needed.
- Now-November: complete 30° sector
  - parasitic operation
  - full track reconstruction
  - output to L3 and private DAQ for L2

  - Without L1CTT: Need to rely on test vectors/ fake data sender
    →Limitations: Less realistic, hard to exercise the whole system (track fits with real SMT hits), timing, data volume, L2 and L3 readout
  - With L1CTT: Easier, Faster

- Full commissioning of the STT will start after installation is complete and all L1CTT inputs are available

- **Run 2B STT can process hit information from 5 of the 6 Run 2B SMT layers**
- **Achieved by adding 1 STC 2 Track Fit Cards per crate**





Conclusions

- **Great progress in board production since Oklahoma**
- **All boards for Run 2a at hand!**
- **Lots of progress in integrating the various pieces**
- **Sector test in progress**
- **All of this made possible by a dedicated STT group**

- **Final System Commissioning coupled to L1CTT schedule.**

- **Run 2b upgrades involve additional STC and TFC boards.**